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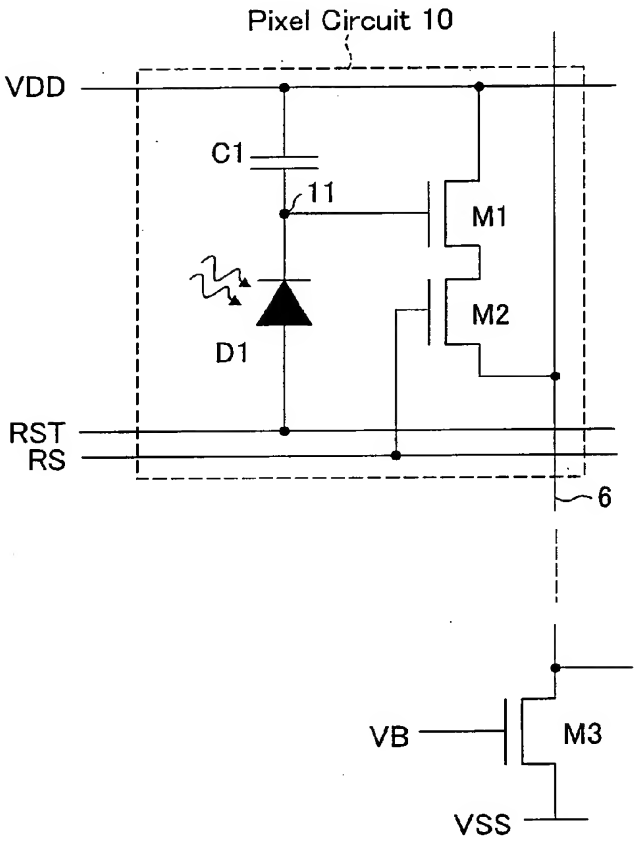
(54) Title: IMAGE SENSOR AND DISPLAY



(57) Abstract: An image sensor, for example for incorporation within an active matrix display, comprises an array of sensor elements 10. Each sensor element (10) comprise an amplifying transistor (M1) whose gate is connected to an integrating node (11). The integrating node (11) is connected to one plate of an integrating capacitor (C1) and to one electrode of a photodiode (D1), whose other electrode is connected to a resetting line (RST). The sensor element (10) performs a repeating sensing cycle comprising a resetting phase, an integrating phase and a reading phase. During the resetting phase, the resetting line (RST) receives a voltage which forward-biases the photodiode (D1) so as to charge the integrating node (11) to a predetermined voltage. The resetting line (RST) is then returned to a voltage for reverse-biasing the photodiode (D1) so that the integrating and reading phases may be performed.

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DESCRIPTION

IMAGE SENSOR AND DISPLAY

TECHNICAL FIELD

The present invention relates to an image sensor and to a display including such an image sensor.

BACKGROUND ART

There is a desire to fabricate an image sensor in a thin-film polysilicon process which is compatible with that used in the manufacture of thin-film transistor substrates for active matrix liquid crystal displays (AMLCDs). By using such a fabrication process, such an image sensor may be monolithically integrated within an AMLCD in order to provide, for example, an input function for detecting a touch or pen input. In such an arrangement, each pixel may include both image sensing and displaying elements to provide similar spatial resolutions of image sensing and display. However, the presence of the image sensing function within the pixels reduces the aperture ratio of such a display as compared with a display in which no image sensing function is provided.

Several types of semiconductor image sensors exist, including those based on charge-coupled device (CCD) technology and those based on complementary metal oxide

silicon (CMOS) technology. CCDs have historically offered higher quality performance than CMOS image sensors because of the specialised process technologies for maximising the transfer efficiency of photo-generated charges. However, CMOS image sensors have an advantage in that both an imaging array and signal processing electronics may be integrated onto the same chip whereas the specialised nature of CCD processes prohibits such integration. CMOS image sensors therefore have advantages of lower cost for many applications, for example in consumer electronics.

Two main types of CMOS image sensors are known, namely passive pixel sensors (PPS) and active pixel sensors (APS). Passive pixel sensors include a photodiode or similar photo sensitive device and a "select" transistor within each pixel of the image sensor. An image sensor array is addressed by row and the current generated by each photodiode is integrated for the duration of one row period by an integrator located typically at the bottom of each column. Because each pixel contains only two active devices, passive pixel arrangements permit a high resolution array to be provided. However, the size of such an array is limited by the time needed to integrate each row sequentially and the output signals suffer from a relatively large degree of noise associated with fluctuations in the column current during integration.

APS devices include an amplifier in each pixel and so do not suffer from the limitations of PPS arrangements. Figure 1 of the accompanying drawings illustrates an example of an APS with a photogate-based pixel circuit, for example as disclosed in US 5,471,515. In operation, during an integration period, electrons accumulate in a potential well beneath a photogate 30 in proportion to a photon flux incident on a substrate beneath the photogate electrode. At the end of each integration period, the potential of a floating diffusion region 40 is reset to an initial level by applying a resetting signal pulse RST. The charge accumulated on the photogate is then transferred to the floating diffusion region 40 during a transfer step controlled by a pulse TX. The potential of the floating diffusion region 40 is thus indicative of the charge accumulated during the integration period.

When a row of pixels is sampled, a row select transistor 60 is turned on by a row scan pulse (ROW). A transistor 55 is connected as a source-follower cooperating with a bias transistor 65 disposed at the end of a column of the pixel array. The gate of the transistor 55 is connected to a floating diffusion node so that the output of the source-follower provides an indication of the voltage at the gate of the transistor 55 and hence of the charge accumulated in the pixel during the integration period.

The image sensor chip also comprises circuitry for

reading out the sampled pixel signal as illustrated at 70 in Figure 1. When the row containing the sensing element is selected, the source follower output voltage representing the incident light intensity is stored in a capacitor 205 via a transistor 200. Transistors 210, 215 and 220 form another source-follower for the column containing the sensing element. When the column select signal COL is pulsed, the output of the column source-follower is supplied to a chip amplifier via an output OUT. The column source-followers are enabled in turn so that the image sensor output voltage is a time-sequential representation of the light intensity incident on each pixel of the array.

The arrangement shown in Figure 1 also comprises devices 116, 225, 230, 235, 240 and 245 which are used to generate a reference voltage for the chip amplifier for reducing offset errors. The operation of such an arrangement is known and will not be described further.

Figure 2 of the accompanying drawings illustrates a sensor element of the APS type including a photodiode 1 of the "bulk" or vertical type, for example as disclosed in "128x128 CMOS photodiode-type active pixel sensor with on-chip timing, control, and signal chain electronics", E Fossum et al, Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE, Vol 2415, pp 117-123, 1995. The sensing element comprises a resetting transistor 2 connected between

a supply line VDD and the cathode 3 of the photodiode 1. The gate of the transistor 2 receives a reset signal RST and reverse-biases the photodiode 1 so as to charge its capacitance to a predetermined voltage. The reset phase is followed by a sensing phase during which integration is performed whereby the photodiode current discharges its capacitance at a rate proportional to the photon flux incident on the photodiode 1. A transistor 4 is connected as a source-follower with its source-drain or "main conduction" path connected in series with that of a selecting transistor 5 between the supply line VDD and a column buss COL BUS 6 of a sensing element array. When a row of pixels is sampled, the row select transistor 5 is turned on by a pulse RS. The column bus is connected to a column reading arrangement, for example of the type illustrated by the transistor 65 and the circuit 70 in Figure 1, to allow the output voltages from the row of pixels to be read out of the sensor.

US 2006/0033729 A1 discloses a device comprising an image sensor integrated within an AMLCD as illustrated in Figure 3 of the accompanying drawings. Each pixel comprises a display portion and an image sensing portion with the latter being of a type similar to that shown in Figure 2 of the accompanying drawings. In this device, each photodiode comprises a thin-film photodiode fabricated using the same process technology as used for manufacture of the AMLCD

thin-film transistor (TFT) substrate. A separate integration capacitor is required in this case because the ratio of the photocurrent to self-capacitance of the thin-film photodiode is large compared to that for a bulk CMOS device. Thus, in the absence of the integration capacitance, the pixel discharge rate would be too high for practical use.

Such a device may be operated in shadow mode or reflection mode. In shadow mode, objects above the AMLCD block the path of ambient light and cast a shadow on the surface of the display, which shadow is detected by the image sensor array. This mode may be used, for example, for touch, pen or gesture input. In reflection mode as illustrated in Figure 4 of the accompanying drawings, light from a display backlight 23 passes through a counter-substrate 24, a liquid crystal layer 25 and a TFT substrate 21 so as to be incident on an object 22 in front of the device. Light reflected from the object 22 returns to the image sensor array for conversion into a corresponding signal. Examples of applications for the reflection mode include contact-type image scanning and fingerprint recognition and identification.

DISCLOSURE OF INVENTION

According to a first aspect of the invention, there is provided an image sensor comprising at least one sensor element, the or each of which comprises a semiconductor

amplifying element, an integrating capacitor, and a photodiode having a first electrode, which is connected to a first control electrode of the amplifying element and a first terminal of the capacitor, and a second electrode connected to a first control input, which is arranged to receive, during a sensing phase, a first voltage for reverse-biasing the photodiode and to receive, during a resetting phase, a second voltage for forward-biasing the photodiode so as to charge the capacitor to a predetermined voltage.

The resetting and sensing phases may be repeated cyclically.

The photodiode may be a lateral photodiode.

The photodiode may be a thin film diode.

The amplifying element may comprise a voltage-follower arrangement.

The amplifying element may comprise a first transistor. The first transistor may be a thin-film transistor. The first transistor may be a field effect transistor. The first transistor may be connected as a source-follower and the first control electrode may comprise the transistor gate.

The sensor may comprise a semiconductor selection element having a main conduction path connected in series with that of the amplifying element and a second control electrode connected to a second control input for controlling selection of the sensor element during a reading phase. The

selection element may comprise a second transistor. The second transistor may be a thin-film transistor.

The capacitor may have a second terminal connected to a second control input, which is arranged to receive, during the sensing phase, a third voltage for disabling the amplifying element and for permitting integration by the capacitor of a photocurrent from the photodiode and to receive, during a reading phase, a fourth voltage for enabling the amplifying element.

The at least one sensor element may comprise a plurality of sensor elements arranged as a first array comprising rows and columns. The sensor may comprise first row control inputs, each of which is connected to the first control inputs of the sensor elements of a respective row. The sensor may comprise second row control inputs, each of which is connected to the second control inputs of the sensor elements of a respective row. The sensor may comprise column outputs, each of which is connected to outputs of the sensor elements of a respective column. Each column output may be connected to a respective biasing element. Each biasing element may comprise a third transistor. Each third transistor may be a thin film transistor.

The sensor may comprise an active matrix addressing arrangement for addressing the sensor elements.

According to a fourth aspect of the invention, there is

provided a display comprising a sensor according to the first aspect of the invention and at least one display pixel.

The at least one pixel may comprise a plurality of pixels arranged as a second array comprising a plurality of the rows and a plurality of the columns. Each of the sensor elements may form part of at least one pixel. The display may comprise pixel column data lines, at least two of which connect the column outputs to the sensor element outputs of the respective columns of sensor elements.

The pixels may be liquid crystal pixels.

The active matrix addressing arrangement may be arranged to address each row of sensor elements during a line blanking period of a corresponding row of pixels.

It is thus possible to provide an image sensor in which each sensor element occupies a reduced area as compared with known arrangements. This may be used, for example, to provide increased "packing density" of sensing elements to provide a sensor of increased spatial resolution. In the case of a combined sensor and display, the sensor elements are of reduced area so that, for a given spatial resolution, a greater portion of pixel area may be used for display purposes, for example to provide a brighter display of improved appearance. For example, such arrangements may be used in devices manufactured using thin-film semiconductor process or silicon-on-insulator (SOI) semiconductor process technologies.

In the case of sensors combined with displays, the aperture ratio, for example of AMLCDs with integrated image sensing, may be substantially increased.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a schematic diagram of part of a known type of image sensor.

Figure 2 is a circuit diagram of a known type of image sensing element.

Figure 3 is a circuit diagram of part of a known display incorporating an image sensor.

Figure 4 is a schematic cross-sectional diagram of a known display including an image sensor operating in reflection mode.

Figure 5 is a circuit diagram of part of an image sensor constituting an embodiment of the invention.

Figure 6 is a circuit diagram illustrating a possible modification of the embodiment shown in Figure 5.

Figure 7 is a circuit diagram illustrating another possible modification of the embodiment shown in Figure 5.

Figure 8 is a circuit diagram of part of an image sensor constituting another embodiment of the invention.

Figure 9 is a timing diagram illustrating waveforms occurring in the embodiment shown in Figure 8.

Figure 10 is a schematic diagram illustrating a display

constituting an embodiment of the invention including an image sensor.

Figure 11 is a diagram illustrating a detail of an example of the embodiment shown in Figure 10.

Figure 12 is a diagram illustrating a detail of another example of the embodiment shown in Figure 10.

Figure 13 is a diagram illustrating a detail of a further example of the embodiment shown in Figure 10.

Figure 14 is a timing diagram illustrating operation of the embodiment shown in Figure 10.

Like reference numerals refer to like parts throughout the drawings.

BEST MODE FOR CARRYING OUT THE INVENTION

An image sensor comprises an array of rows and columns of sensor elements, each of which is as illustrated at 10 in Figure 5. The sensor elements 10 together with addressing and output circuits are integrated on a common substrate, for example using thin-film transistor or silicon-on-insulator techniques. The sensor comprises an active matrix device, which may be combined with an active matrix display of the liquid crystal type as described hereinafter.

The sensor element 10 comprises a photodetector in the form of a lateral thin-film photodiode D1. The anode of the photodiode D1 is connected to a reset line RST which is

common to all of the sensor elements in the same row. The cathode of the photodiode D1 is connected to an integrating node 11, which is connected to the first electrode or plate of an integrating capacitor C1, whose other electrode or plate is connected to a supply line VDD.

The sensing element 10 comprises a semiconductor amplifying element in the form of a thin-film insulated gate field effect transistor M1 arranged as a source-follower with its gate connected to the cathode of the photodiode D1 and the first electrode of the capacitor C1, its drain connected to the supply line VDD, and its source providing an output signal. The source-drain path of the transistor M1 is connected in series with the source-drain path of another insulated gate field effect transistor M2 between the supply line VDD and a column output line 6. The gate of the transistor M2 is connected to a row select line RS, which is common to the sensor elements in the same row. The source of the transistor M2 forms an output of the sensing element 10 with the outputs of the sensing elements in the same column being connected to the same column output line 6.

The end of the column output line 6 is connected to the drain of an insulated gate field effect transistor M3, whose source is connected to another supply line VSS and whose gate is connected to a reference voltage generator via a reference voltage line VB. The transistor M3 acts as a biasing

element forming an active source load for the transistor M1 of each sensor element 10 of the column currently selected for reading. The drain of the transistor M3 comprises the column output and is connected to an output reading circuit of any suitable type, for example of the type as described hereinbefore with reference to Figure 1.

Each of the sensor elements 10 performs a repeating cycle of operation having various phases. At the start of a sensing phase which comprises an integration period, a pulse is supplied to the reset line RST so as to forward-bias the photodiode D1. The photodiode D1 thus conducts so as to set the voltage across the capacitor C1 to a predetermined initial value. For example, the voltage of the reset line RST is normally at V_{SS}, which is the voltage of the supply line VSS and is typically zero volts. The pulse has an amplitude equal to V_{DD} so that the initial voltage across the capacitor C1 is equal to the supply line voltage V_{DD} minus the forward voltage drop across the photodiode D1. Following resetting, the voltage of the reset line RST returns to the value V_{SS} so that the photodiode D1 is reverse-biased.

During the integration period, the photodiode current discharges the integration capacitor C1 at a rate proportional to the photon flux incident on the photodiode. At the end of the integration period, the voltage across the capacitor C1 has fallen by an amount equal to the product of the photodiode

current and the integration period time divided by the capacitance of the capacitor C1 (in parallel with the capacitance of the photodiode D1 and the gate capacitance of the transistor M1).

At the end of the integration period, a row select pulse is supplied to the row select line RS. The voltage supplied to the gate of the transistor M2 thus rises from below the transistor threshold voltage to above the transistor threshold voltage in order to switch on the transistor M2. The source of the transistor M1 is thus connected via the control line 6 to the drain of the bias transistor M3 to form a source-follower, which acts as a voltage-follower arrangement. The output voltage of the source-follower provides a measure of the photodiode current integrated during the integration period and hence of the intensity of light incident on the photodiode D1.

The sensor element 10 occupies less area than known arrangements while allowing the whole element to be formed using thin-film or silicon-on-insulator techniques. For example, the sensor element 10 of Figure 5 requires only two transistors as compared with the three transistors required in the known arrangement shown in Figure 3. This allows a low cost image sensor to be manufactured with more sensor elements per unit area to provide increased spatial resolution of image sensing. Alternatively, when the sensor forms part

of a display, the area occupied by the sensor elements is reduced so that the aperture ratio of the display may be increased, for example as compared with the arrangement shown in Figure 3. Thus, improved brightness and quality of display may be achieved as compared with known arrangements.

The sensor element 10 shown in Figure 6 differs from that shown in Figure 5 in that the polarity of the photodiode D1 is reversed so that the cathode is connected to the reset line RST whereas the anode is connected to the integrating node 11. Also, the reset line RST normally carries the voltage V_{DD} of the supply line VDD and a reset pulse causes this voltage to fall to the voltage V_{SS} of the supply line VSS. The operation of the sensor element 10 is similar to the operation of the element shown in Figure 5. However, during the reset phase, the potential of the integrating node formed by the first plate of the capacitor C1 is set to the voltage V_{SS} plus the forward voltage drop across the photodiode D1 and rises during the integration period at a rate determined by the capacitance which is present at the integrating node 11 and by the photocurrent through the photodiode D1.

Figure 7 illustrates a modification to the sensor element of Figure 5, which modification may also be applied to the sensor element Figure 6. In particular, a light shield 11a is provided above the photodiode D1 and is connected to the

integrating node 11 of the sensor element 10.

The use of such a light shield 11a is necessary, for example when the sensor element 10 is part of a display, such as an AMLCD. In such a case, the display substrate is transparent and exposed to a backlight in addition to the ambient light to be sensed. The light shield 11a may, for example, be fabricated in any suitable layer of a TFT process and is arranged to block light from the backlight entering a photosensitive region of the photodiode D1 so that substantially only the incident ambient light contributes to the photodiode current.

Figure 8 illustrates a sensor element of an image sensor which requires only one transistor M1 and thus occupies an even smaller substrate area, permitting even greater image sensing spatial resolution and/or display aperture ratio. The source-follower transistor M1 and the biasing transistor M3 are as described hereinbefore. The cathode of the photodiode D1 and the first electrode (terminal) of the integrating capacitor C1 are connected to the integrating node 11 and to the gate of the transistor M1. The anode of the photodiode D1 is connected to the reset line RST. The second electrode (terminal) of the capacitor C1 is connected to the row select line RS and the transistor M2 is omitted. The waveforms on the resetting line RST and on the row select RS are illustrated by the upper and lower waveforms shown in Figure 9.

As described hereinbefore, the sensor elements perform a repeating cycle of resetting, integrating and reading phases. The cycles are synchronised with each other for the sensor elements 10 in the same row and the cycles for different rows are staggered or offset in time, for example in accordance with known active matrix addressing techniques.

At the start of the resetting phase, the signal on the resetting line RST rises to its higher level of V_{DDR}. The photodiode D1 thus becomes forward-biased and conducts so as to charge the integration mode 11 to a potential of (V_{DDR}-V_D), where V_D is the forward voltage of the photodiode. The voltage V_{DDR} is less than the threshold voltage of the transistor M1 so that this transistor remains switched off during the resetting phase and during the subsequent integrating phase.

The integrating phase begins when the resetting signal returns to its low value. During this phase, the photodiode current discharges the integration capacitor C1 at a rate proportional to the photon flux incident on the photodiode. At the end of the integration phase (when the row is selected for reading), the voltage V_{INT} at the integrating node 11 is given by:

$$V_{INT} = V_{DDR} - V_D - I_{PHOTO}.t_{INT}/C_T$$

where I_{PHOTO} is the current through the photodiode D1, t_{INT} is the integration time period and C_T is the total

capacitance at the integrating node 11. The total capacitance C_T is the total of the capacitance of the capacitor C_1, the self-capacitance of the photodiode D1 and the gate capacitance of the transistor M1.

At the start of the reading phase, the row select signal on the line RS rises to its higher value. Charge injection occurs across the integrating capacitor C1 such that the potential at the integrating node 11 is increased to:

$$V_{INT} = V_{DDR} - V_D - I_{PHOTO}.t_{INT}/C_T + (V_{RS.H} - V_{RS.L}).C_{INT}/C_T$$

where $V_{RS.H}$ and $V_{RS.L}$ are the high and low potentials, respectively, of the row select signal and may be equal to V_{DD} and V_{SS}, respectively.

The potential at the integrating node 11 thus rises above the threshold voltage of the source-follower transistor M1 such that it operates, together with the bias transistor M3 at the end of the column, as a source-follower amplifier. The output voltage supplied to the column output represents the photodiode current integrated during the integration phase and so represents the intensity of light incident on the photodiode D1.

At the end of the reading phase, the row select signal on the line RS returns to its low value. Charge is removed from the integrating node 11 by charge injection across the capacitor C1. The potential of the integrating node 11 thus drops below the threshold voltage of the transistor M1, which

is thus turned off.

As mentioned hereinbefore, the second terminal of the capacitor C1 is connected to the supply line (second control input) VDD in the form of the row select line RS. During the sensing or integrating phase, the row select line RS receives a voltage (third voltage) VDDR/VSS, which disables the amplifying element M1 and permits integration of the photocurrent. During the reading phase at the end of the integration period, as shown in the lower graph of Figure 9, the row select line RS receives the voltage (fourth voltage) V_{DD}, which enables the transistor M1 by causing, by charge injection, the gate of the transistor M1 to rise above the transistor threshold voltage to a voltage determined at least in part by the light incident on the photodiode D1 during the integration period.

As mentioned hereinbefore, the substrate area occupied by the sensor element 10 of Figure 8 is even less than that of the previously described embodiments by the omission of the row select transistor M2.

As mentioned hereinbefore, the array of sensor elements 10 and the output circuitry at the bottom of the columns may be incorporated within a display so as to provide such a display with an input facility, for example in the form of a "touch screen". Figure 10 illustrates the layout of such a device on a common substrate, on which all of the

components are integrated, for example by thin-film technology or silicon-on-insulator technology. A transparent substrate 12, for example made of glass, carries a pixel matrix 13 comprising an array or matrix of display picture elements (pixels) including the sensor elements, together with appropriate electrodes extending in the row and column directions. The display receives image data together with timing signals and power from any suitable image source and comprises a display source driver 14 and a display gate driver 15. Such drivers are known in the field of active matrix devices and will not therefore be described further. The device also comprise a sensor row driver 16 and a sensor read-out driver 17. The drivers 16 and 17 receive timing and power signals from apparatus for processing the sensor data. The sensor read-out driver 17 may be of conventional type as described hereinbefore and the sensor row driver 16 may be similar to the display gate driver 15.

Figure 11 illustrates an example of the combined display and sensor arrangement of Figure 10 in the form of an active matrix liquid crystal display (AMLCD) including the image sensing function. The circuit diagram of one of the pixel circuits 18 forming the array is shown in detail. The display pixel is of known type and comprises a thin-film insulated gate field effect transistor M4 whose gate is connected via a row gate line GL to the display gate driver 15 and whose

source is connected via a column source line SL to the display source driver 14. The drain of the transistor M4 is connected to one electrode of a capacitor C2 and to one electrode of a liquid crystal pixel CLC. The other electrode of the capacitor C2 is connected via a common line TFTCOM to the driver 15. The other pixel electrode is constituted by a counter-electrode on the opposite device substrate connected to receive a common counter-electrode voltage VCOM.

The sensor element 10 is of the type illustrated in Figure 8 and comprises the single transistor M1, the thin-film lateral photodiode D1 and the integrating capacitor C1. The supply line VDD and the column output line 6 are connected to the sensor read-out driver 17. The row select line RS and the reset line RST are connected to the sensor row driver 16.

The operation of the image display pixels in such an AMLCD is well-known and will not be described further. The operation of the image sensor comprising the sensor elements 10 and the drivers 16 and 17 is as described hereinbefore. Although the addressing of the display pixels and the sensor elements may be performed independently, such addressing is generally synchronised on a row-by-row basis and an example of the timing of such addressing is described hereinafter.

In the display of Figure 11, each sensor element 10 is disposed within each pixel circuit 18 so that the image sensing spatial resolution is the same as the image display

spatial resolution. However, the sensing and display resolutions need not be the same and each may be chosen according to the needs of any particular application. For example, Figure 12 illustrates a display in which one sensor element 10 is provided for each set of three colour component pixels forming a composite full-colour pixel. Separate source lines SLr, SLg and SLb are provided for the RGB component pixels of each column of composite pixels. The photodiode D1 and the integrating capacitor C1 are disposed within one of the colour component pixels, in this case the red pixel, whereas the transistor M1 is disposed within the green colour component pixel. This reduces the area occupied by the sensor element circuitry within each colour component pixel and thus increases the lowest pixel aperture ratio. Locating the photodiodes D1 under colour component pixels of one colour would make the image sensor sensitive to monochromatic light of that colour. This may be avoided by locating the photodiodes under different colour filter colours across the device or by operating the device with the active matrix substrate uppermost, for example as illustrated in Figure 4. In the arrangement of Figure 4, ambient light does not pass through the display colour filtering before being incident on the photodiodes.

Figure 13 illustrates a display which differs from that of Figure 12 in that the source lines are also used as the column

output lines 6 of the image sensor so as to increase even further the lowest pixel aperture ratio. Because of the sharing of the lines as source lines and column output lines, it is necessary for addressing or scanning of the image display pixels and the sensor elements to be performed with the appropriate timing and an example of such timing is illustrated in the waveform diagram of Figure 14. The reading phase of each sensor element row need only be performed for a relatively small portion of the total row addressing time of each row and this may be arranged to coincide with the horizontal blanking period of the display function, during which time the source lines are normally disconnected from the display source driver 14.

As illustrated in Figure 14, each display row period starts with a horizontal sync pulse HSYNC, after which the source lines SLr, SLg and SLb are driven with suitable voltages in order to control the optical states of the colour component pixels of the selected row so as to refresh the image row-by-row as in known addressing schemes.

Following signal transfer to the image display pixels of the row, the source lines are disconnected from the display source driver 14 at the start of the blanking period, which is commonly used in known AMLCDs to invert the polarity of the counter-electrode so as to prevent degradation of the liquid crystal material. During the blanking period, the sensor

element row select signal rises on the line RS and the bias voltage VB is applied to the transistors M3 to which the column output lines 6 are connected so as to enable the source-follower arrangement in the image elements of the currently selected row. The sensor data are thus output via the column lines SLg to the sensor read-out driver 17, which acts as an interface between the sensor elements 10 and the sensor output of the device.

At the end of the reading phase of the selected row of sensor elements, the row select and bias signals return to their low potential. A resetting signal is applied to the reset line RST for the sensor elements of the selected row so as to reset the integrating nodes to the predetermined voltage. The resetting signal is then removed at the end of the row addressing period t_{ROW} and the process is then repeated for the next pixel row.

The arrangement illustrated in Figure 13 gives one example of spreading the sensor element components across a plurality of pixels to increase the lowest pixel aperture ratio and of sharing common lines to reduce the area occupied by the sensor element and thus increase the aperture ratio of the display. However, the components of the sensor elements may be arranged in any other suitable manner across the display pixels. Also, other common line sharing arrangements are possible.

CLAIMS

1. An image sensor comprising at least one sensor element, the or each of which comprises a semiconductor amplifying element, an integrating capacitor, and a photodiode having a first electrode, which is connected to a first control electrode of the amplifying element and a first terminal of the capacitor, and a second electrode connected to a first control input, which is arranged to receive, during a sensing phase, a first voltage for reverse-biasing the photodiode and to receive, during a resetting phase, a second voltage for forward-biasing the photodiode so as to charge the capacitor to a predetermined voltage.

2. A sensor as claimed in claim 1, in which the resetting and sensing phases are repeated cyclically.

3. A sensor as claimed in claim 1 or 2, in which the photodiode is a lateral photodiode.

4. A sensor as claimed in any one of the preceding claims, in which the photodiode is a thin film diode.

5. A sensor as claimed in any one of the preceding claims, in which the amplifying element comprises a voltage-

follower arrangement.

6. A sensor as claimed in any one of the preceding claims, in which the amplifying element comprises a first transistor.

7. A sensor as claimed in claim 6, in which the first transistor is a thin film transistor.

8. A sensor as claimed in claim 6 or 7, in which the first transistor is a field effect transistor.

9. A sensor as claimed in claim 8 when dependent on claim 5, in which the first transistor is connected as a source-follower and the first control electrode comprises the transistor gate.

10. A sensor as claimed in any one of the preceding claims, comprising a semiconductor selection element having a main conductive path connected in series with that of the amplifying element and a second control electrode connected to a second input for controlling selection of the sensor element during a reading phase.

11. A sensor as claimed in claim 10, in which the

selection element comprises a second transistor.

12. A sensor as claimed in claim 11, in which the second transistor is a thin film transistor.

13. A sensor as claimed in any one of claims 1 to 9, in which the capacitor has a second terminal connected to a second control input, which is arranged to receive, during the sensing phase, a third voltage for disabling the amplifying element and for permitting integration by the capacitor of a photocurrent from the photodiode and to receive, during a reading phase, a fourth voltage for enabling the amplifying element.

14. A sensor as claimed in any one of the preceding claims, in which the at least one sensor element comprises a plurality of sensor elements arranged as a first array comprising rows and columns.

15. A sensor as claimed in claim 14, comprising first row control inputs, each of which is connected to the first control inputs of the sensor elements of a respective row.

16. A sensor as claimed in claim 14 or 15, when dependent on any one of claims 10 to 13, comprising second

row control inputs, each of which is connected to the second control inputs of the sensor elements of a respective row.

17. A sensor as claimed in any one of claims 14 to 16, comprising column outputs, each of which is connected to outputs of the sensor elements of a respective column.

18. A sensor as claimed in claim 17, in which each column is connected to a respective biasing element.

19. A sensor as claimed in claim 18, in which each biasing element comprises a third transistor.

20. A sensor as claimed in claim 19, in which each third transistor is a thin film transistor.

21. A sensor as claimed in any one of claims 14 to 20, comprising an active matrix addressing arrangement for addressing the sensor elements.

22. A display comprising a sensor as claimed in any one of the preceding claims and at least one display pixel.

23. A display as claimed in claim 22 when dependent on any one of claims 14 to 21, in which the at least one pixel

comprises a plurality of pixels arranged as a second array comprising a plurality of the rows and a plurality of the columns.

24. A display as claimed in claim 23, in which each of the sensor elements forms part of at least one pixel.

25. A display as claimed in claim 23 or 24 when dependent directly or indirectly on claim 17, comprising pixel column data lines, at least two of which connect the column outputs to the sensor element outputs of the respective columns of sensor elements.

26. A display as claimed in any one of claims 23 to 25, in which the pixels are liquid crystal pixels.

27. A display as claimed in any one of claims 23 to 26 when dependent on claim 21, in which the active matrix addressing arrangement is arranged to address each row of sensor elements during a line blanking period of a corresponding row of pixels.

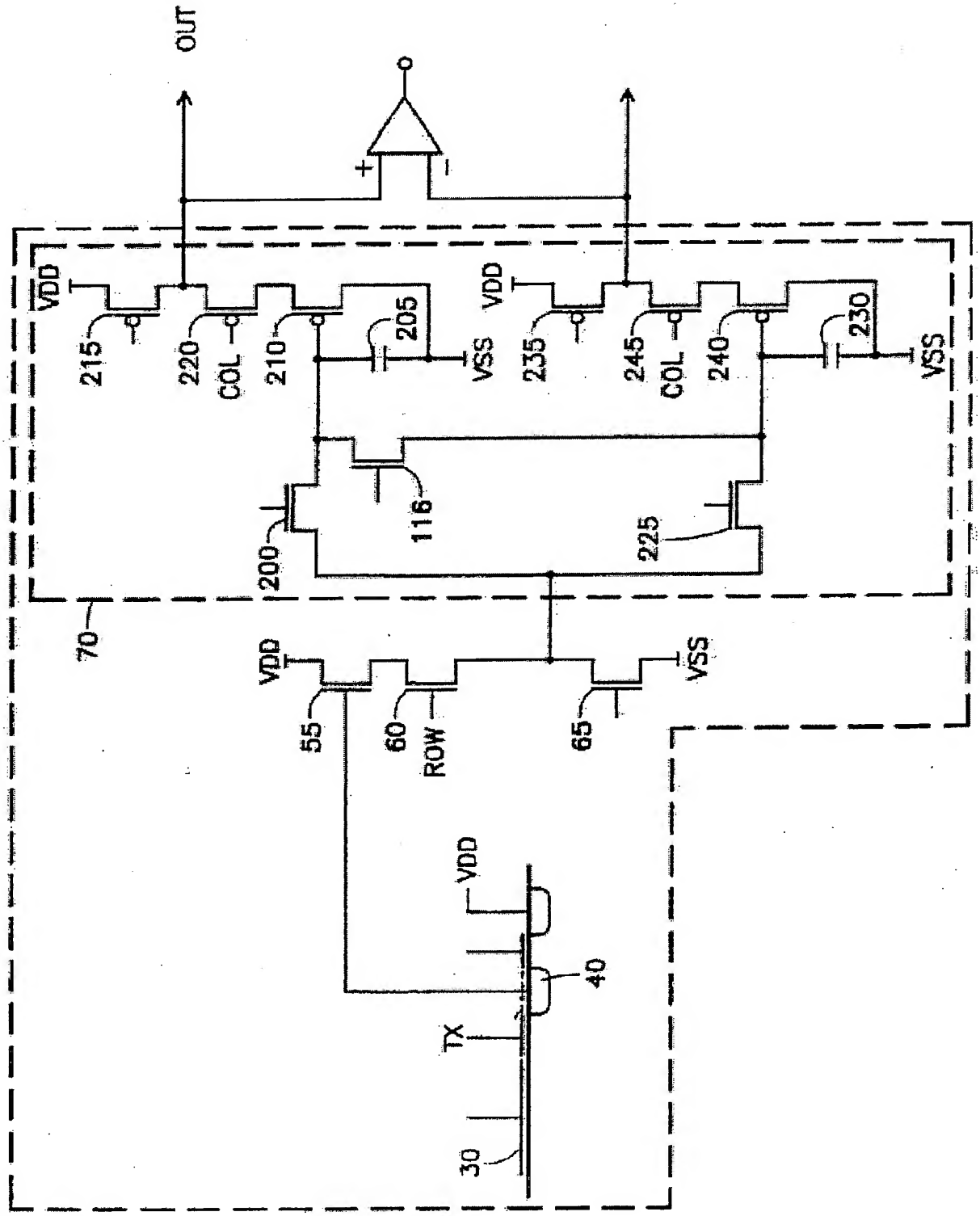


FIG. 1
Prior Art

FIG. 2

Prior Art

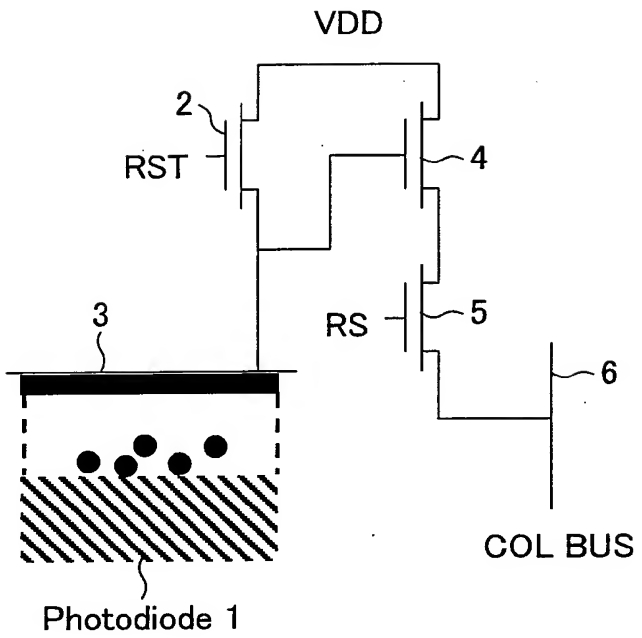


FIG. 3

Prior Art

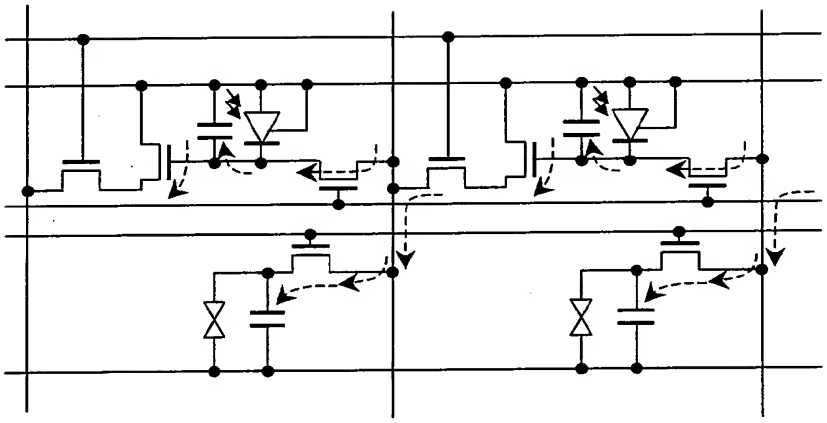


FIG. 4

Prior Art

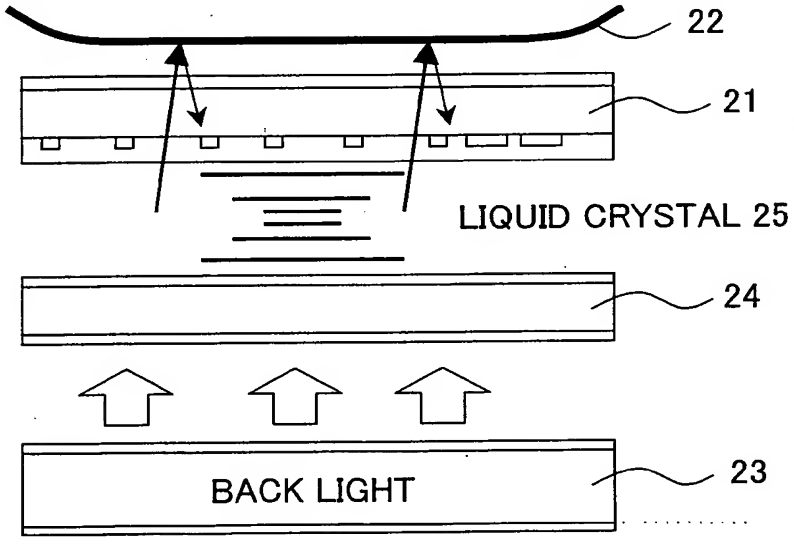


FIG. 5

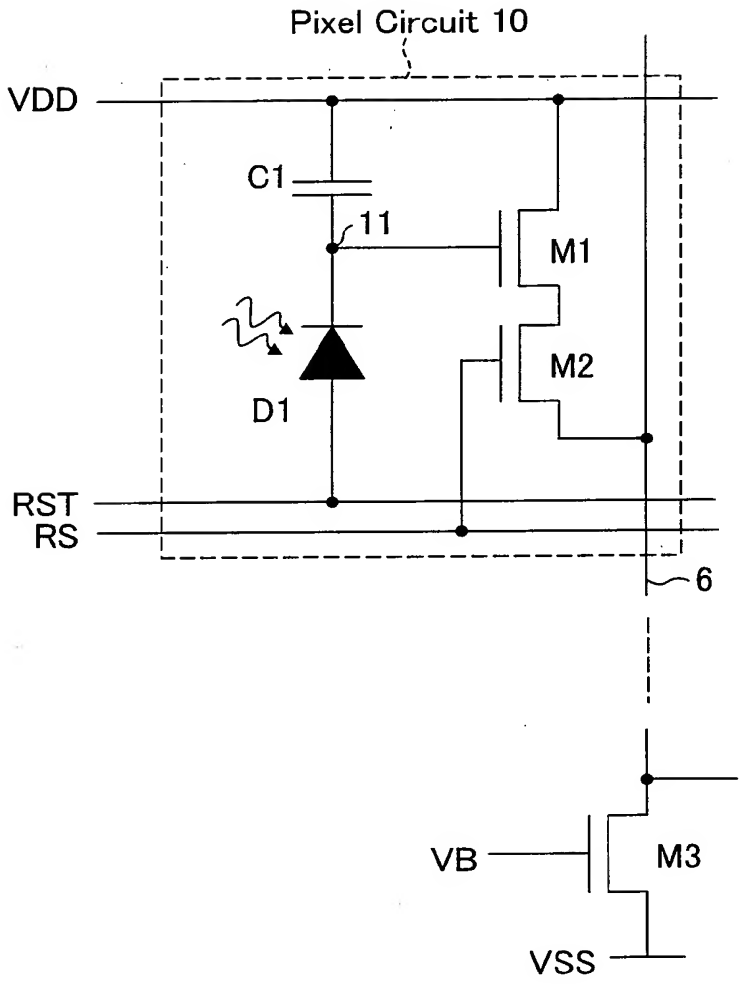


FIG. 6

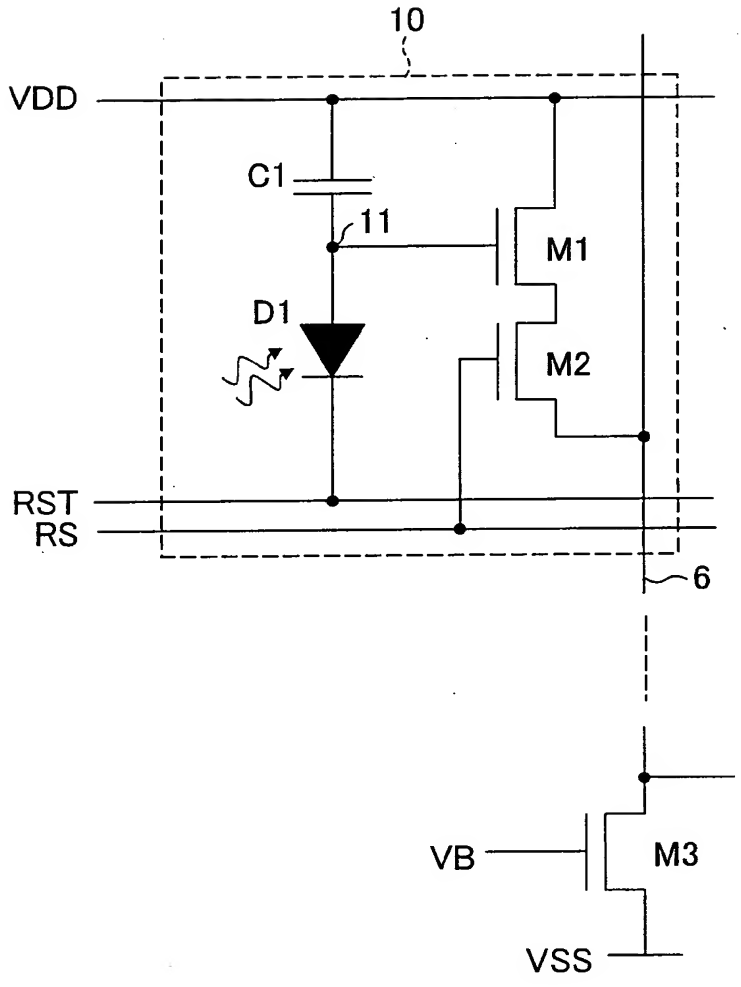


FIG. 7

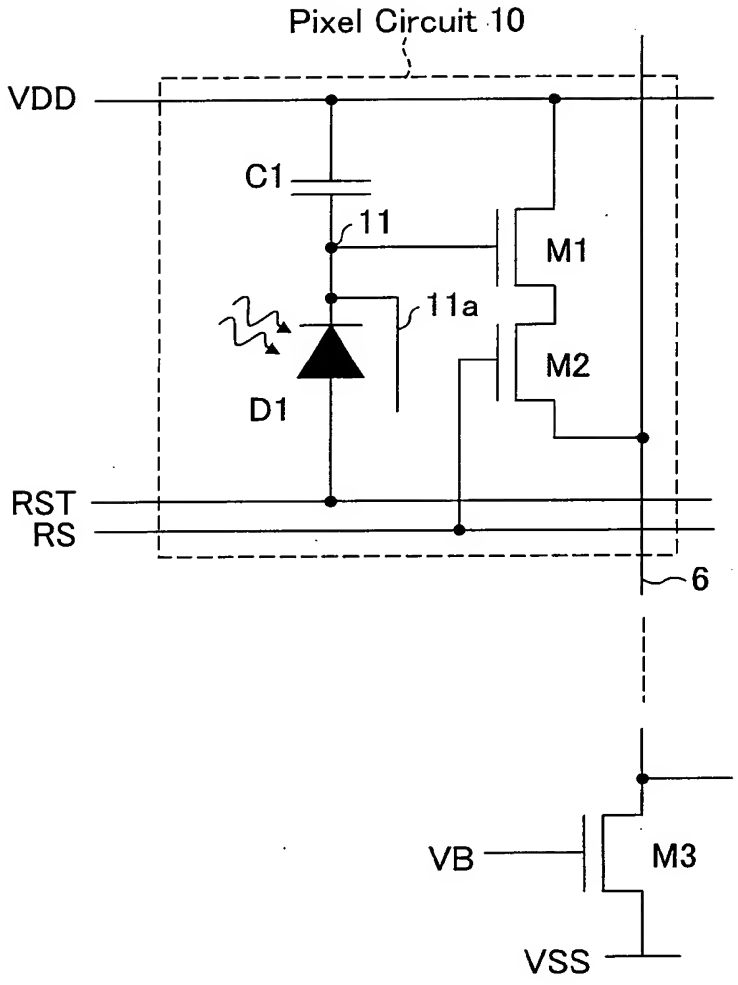


FIG. 8

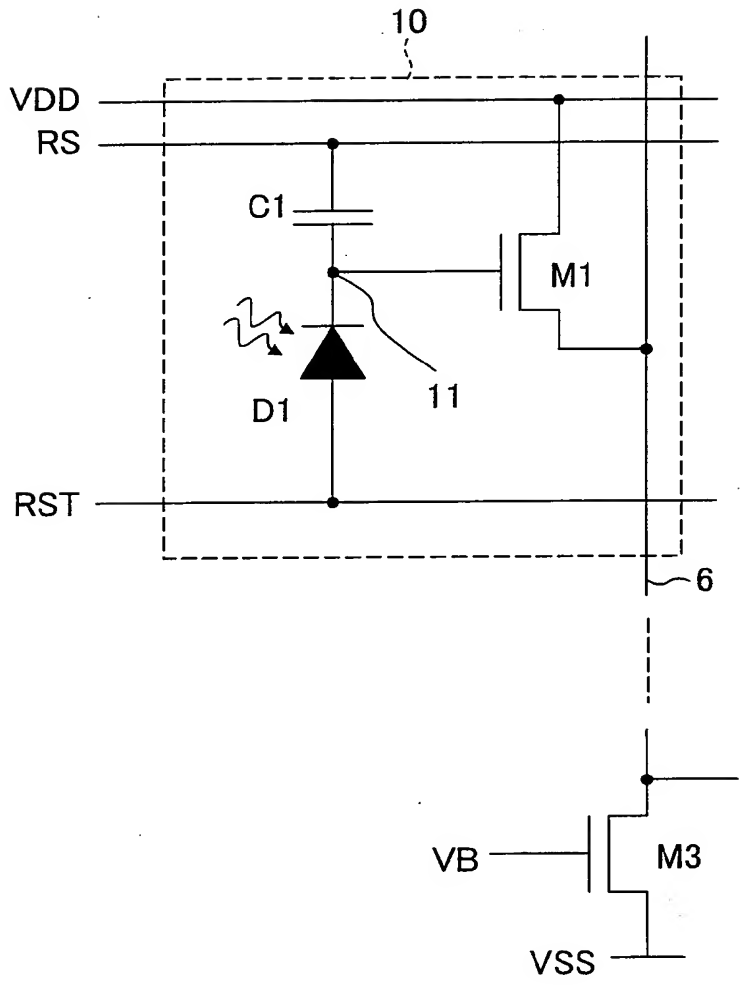


FIG. 9

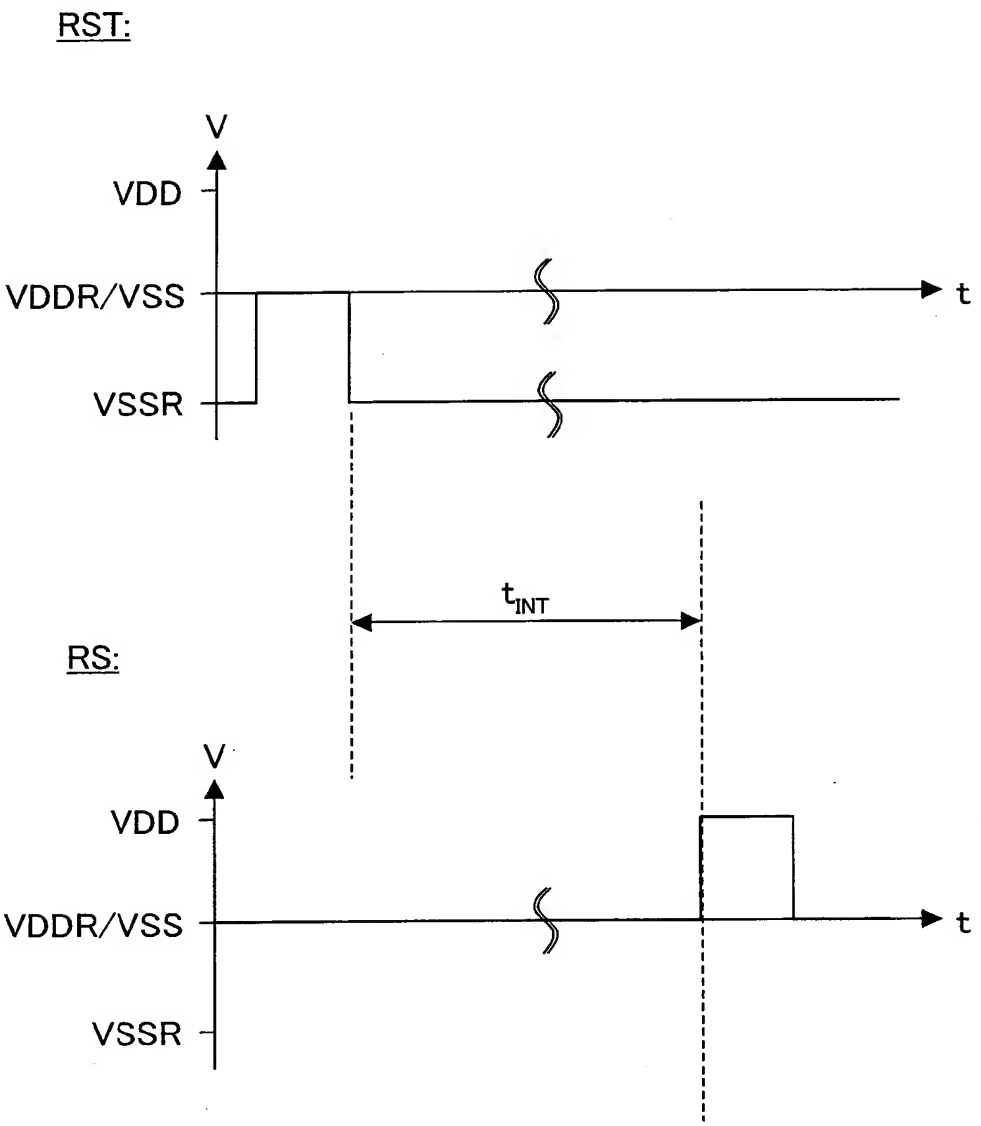


FIG. 10

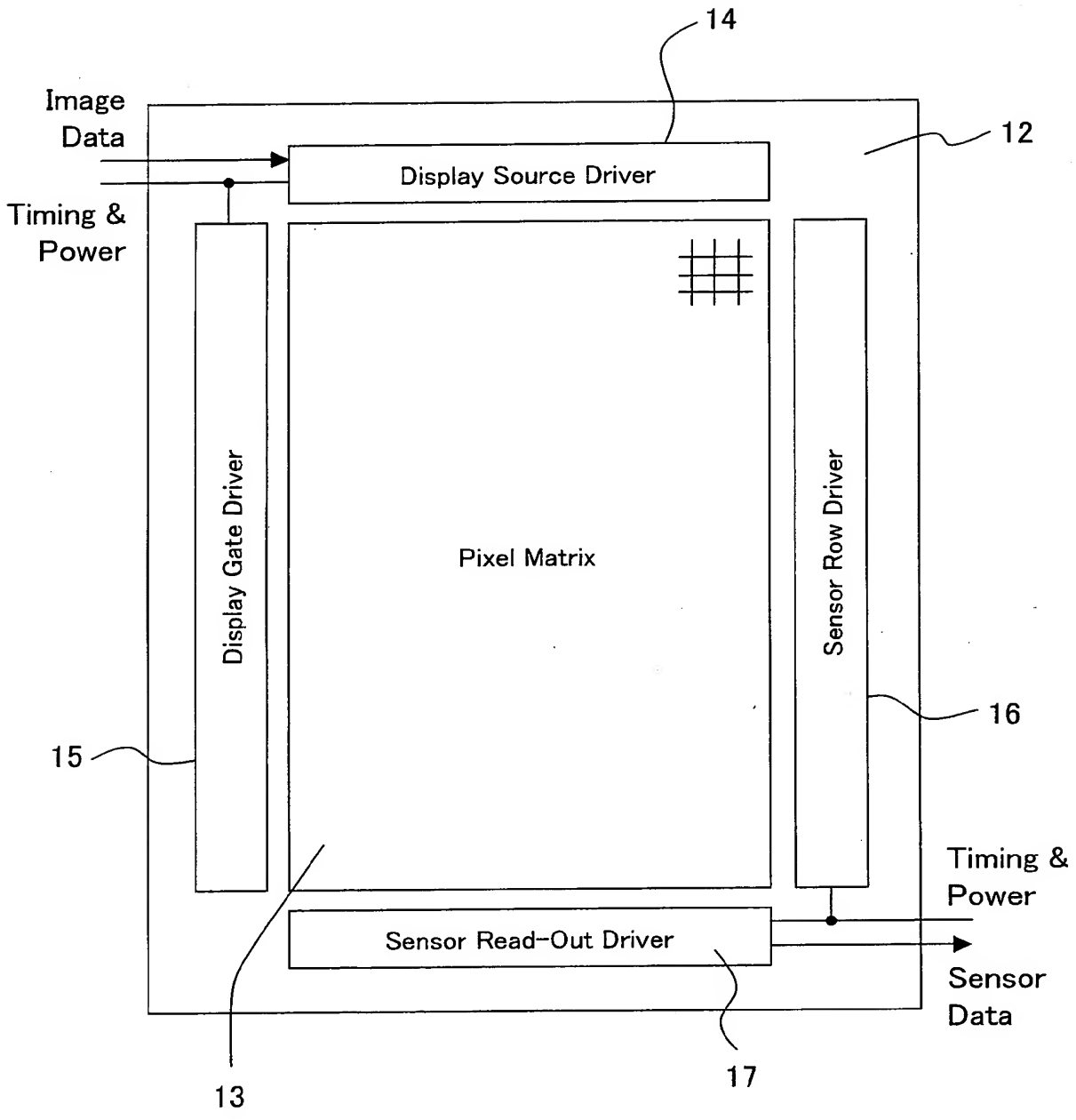

14
Image Data
12
Display Source Driver
Timing & Power
Display Gate Driver
Pixel Matrix
Sensor Row Driver
16
15
Timing & Power
Sensor Read-Out Driver
Sensor Data
13
17

FIG. 11

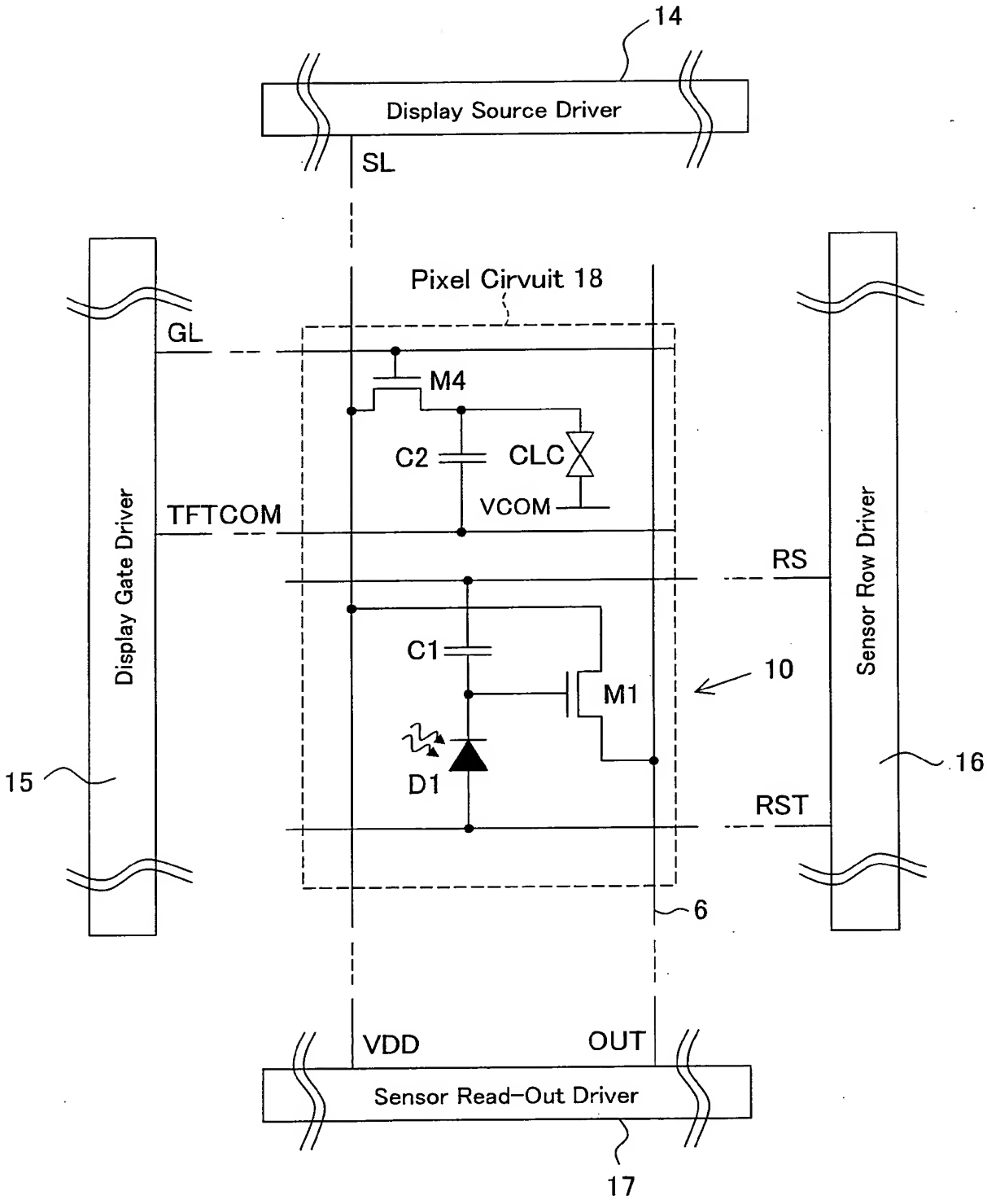

14
Display Source Driver
SL
Pixel Cirvuit 18
GL
M4
C2
CLC
VCOM
TFTCOM
RS
C1
M1
10
D1
RST
Display Gate Driver
Sensor Row Driver
15
16
6
VDD
OUT
Sensor Read-Out Driver
17

FIG. 12

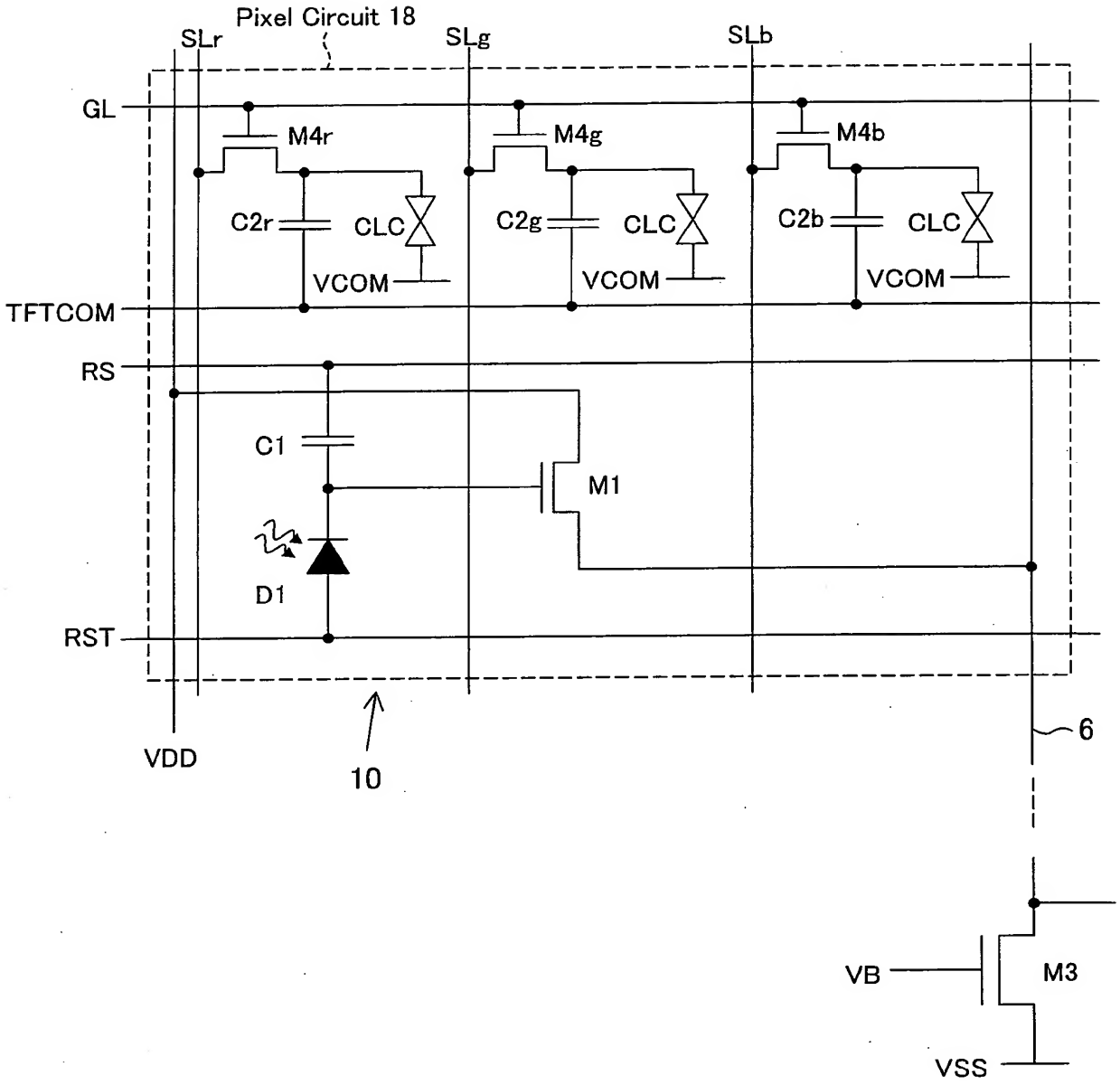

Pixel Circuit 18
SLr
SLg
SLb
GL
M4r
M4g
M4b
C2r
CLC
VCOM
C2g
CLC
VCOM
C2b
CLC
VCOM
TFTCOM
RS
C1
M1
D1
RST
VDD
10
6
VB
M3
VSS

FIG. 13

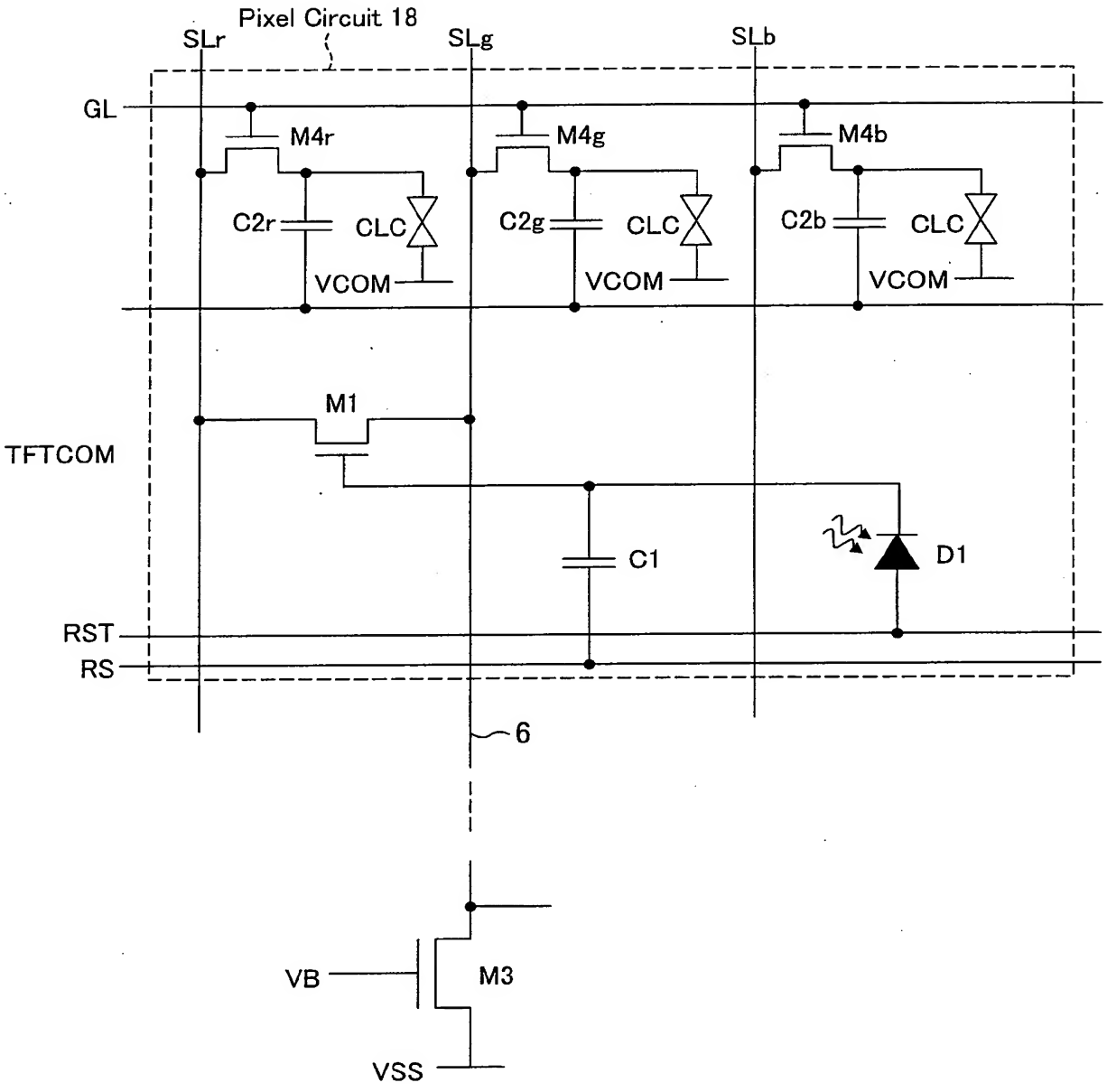
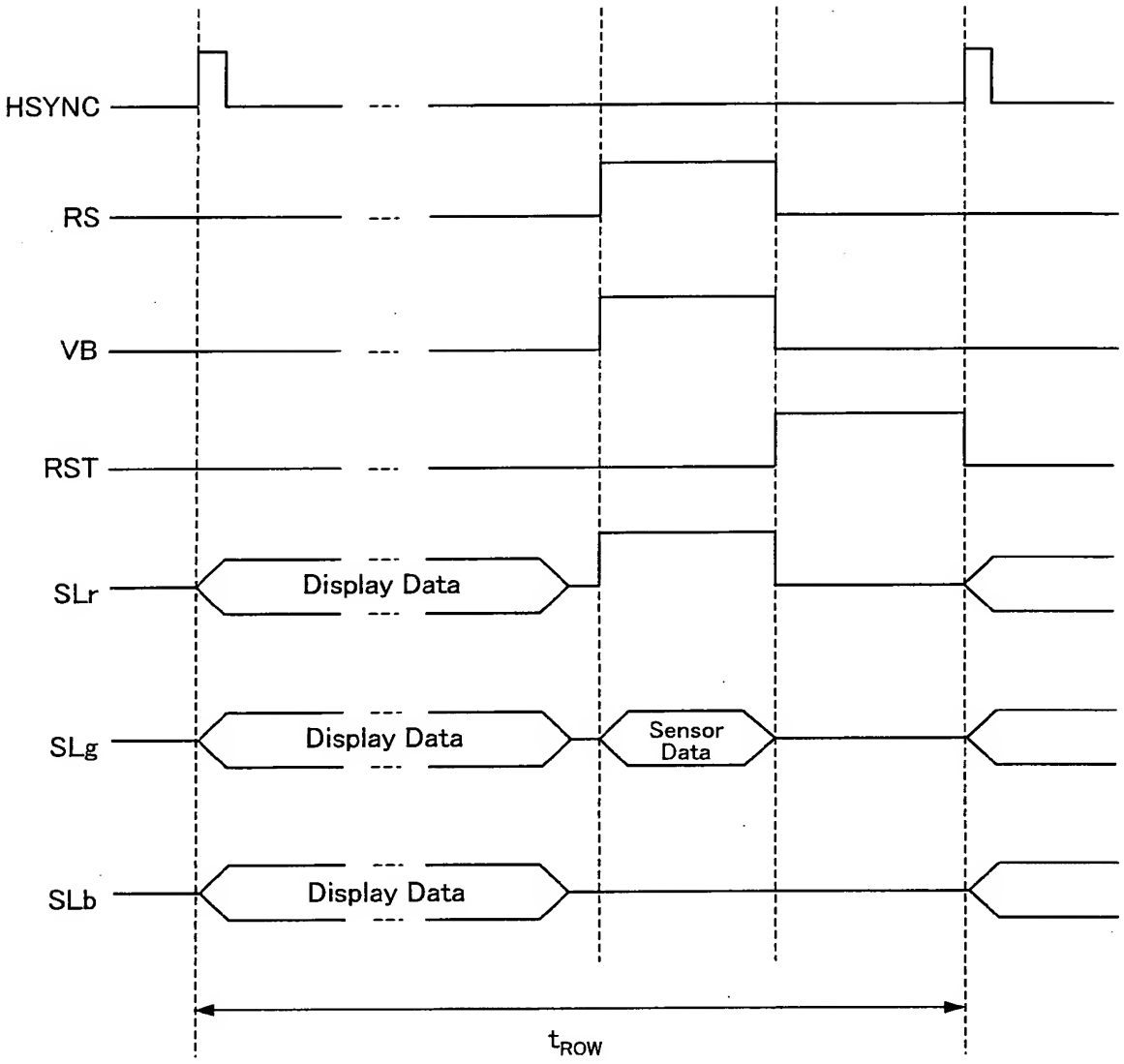

Pixel Circuit 18
SLr
SLg
SLb
GL
M4r
M4g
M4b
C2r
CLC
C2g
CLC
C2b
CLC
VCOM
VCOM
VCOM
M1
TFTCOM
C1
D1
RST
RS
6
VB
M3
VSS

FIG. 14


HSYNC
RS
VB
RST
SLr
Display Data
SLg
Display Data
Sensor Data
SLb
Display Data
t_{ROW}

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2007/062184

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04N5/335(2006.01)i, G02F1/1368(2006.01)i, G06F3/041(2006.01)i, G09G3/20(2006.01)i, G09G3/36(2006.01)i, H01L27/146(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04N5/335, G02F1/1368, G06F3/041, G09G3/20, G09G3/36, H01L27/146

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applicatcns of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2007
Registered utility model specifications of Japan 1996-2007
Published registered utility model applications of Japan 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-177886 A (SHARP KABUSHIKI KAISHA) 1999.07.02, paragraphs [0001]-[0090], Fig.1-13 & US 6163023 A	1-27
A	JP 9-247536 A (KABUSHIKI KAISHA TOSHIBA) 1997.09.19, paragraphs [0029]-[0069], Fig.1-4 (Family: none)	1-27
A	JP 2004-318067 A (Toshiba Matsushita Display Technology Co., Ltd.) 2004.11.11, paragraphs [0001]-[0125], Fig.1-15 (Family: none)	22-27
A	JP 2004-45879 A (Toshiba Matsushita Display Technology Co., Ltd.) 2004.02.12, paragraphs [0001]-[0072], Fig.1-16 & US 2004/0008172 A1	22-27

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06.09.2007	18.09.2007

Name and mailing address of the ISA/JP	Authorized officer
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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2007/062184

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2004-318819 A (Toshiba Matsushita Display Technology Co., Ltd.) 2004.11.11, paragraphs [0001]-[0112], Fig.1-33 & US 2006/0192766 A1 & EP 1610210 A1 & WO 2004/088496 A1	1-27
A	JP 2002-314756 A (SHARP KABUSHIKI KAISHA) 2002.10.25, paragraphs [0001]-[0069], Fig.1-13 (Family: none)	22-27